



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,036	08/20/2003	Yu-Seock Yang	P-0576	5075

34610 7590 05/30/2007  
KED & ASSOCIATES, LLP  
P.O. Box 221200  
Chantilly, VA 20153-1200

EXAMINER
----------

LEADER, WILLIAM T

ART UNIT	PAPER NUMBER
----------	--------------

1742

MAIL DATE	DELIVERY MODE
-----------	---------------

05/30/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/644,036

**Applicant(s)**

YANG ET AL.

**Examiner**

William T. Leader

**Art Unit**

1742

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. Receipt of the papers filed on March 3, 2007, is acknowledged. Claims 2-19 are pending.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. The amendment to claim 8 has overcome the rejection under 35 U.S.C. 112, second paragraph.

#### ***Claim Rejections - 35 USC § 102***

4. Claims 2-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese patent publication 2001-110939, hereinafter Hirobumi et al, for the reasons given in the previous office action and in view of the following comments.

#### ***Claim Rejections - 35 USC § 103***

5. Claims 8-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art combined with Japanese patent publication 2001-110939, hereinafter Hirobumi et al, for the reasons given in the previous office action and in view of the following comments.

*Response to Arguments*

6. Applicant's arguments have been fully considered but they are not deemed to be persuasive. At page 11 of the Remarks, applicant argues that Hirobumi et al does not disclose or suggest the limitations in the combination of claim 2 and, in particular, argues that Hirobumi et al does not disclose or suggest supplying power to the connection pads through a power connection portion. These arguments are not convincing. Independent claim 2, as well as independent claims 9 and 19, recites "using some of the circuit patterns provided in the substrate as a power connection portion". The flow of electric current to cause metal to be electroplated onto bonding pad 64 is shown in applicant's figure 4H. The current flows through conductive layer 78 on the side of the circuit board opposite to that on which bonding pad 64 is located, through the through-hole 58 which was metallized as shown in figure 4B, and through metal layer 68 to pad 64 which is exposed to the plating solution through an opening in photoresist 70. In Hirobumi et al, the flow of electric current to cause metal to be electroplated onto the bonding pad on the top (component) side of the circuit board is the same as that recited by applicant. The current flows through conductive layer 5 (corresponding to applicant's layer 78) on the side of the circuit board opposite to that on which the bonding pad is located, through the metallized through-hole 3, through the copper circuit pattern on the top side of the board to bonding pad which is exposed to the plating solution through an opening in resist 4.

7. At page 11 applicant points out that Hirobumi et al disclose the use of the non-electrolytic copper as a flow object for partial electrolytic plating. This is correct, but is the same procedure used by applicant. Applicant deposits resist 70 over the copper circuit patterns on the

circuit board, and then layer 78 on the bottom side of the circuit board over resist 70. See figure 4E. Layer 78 may be deposited by non-electrolytic processes such as electroless plating or sputtering (page 9, lines 24-25 of applicant's specification). Hirobumi et al deposits resist 4 (corresponding to applicant's resist 70) over copper circuit patterns 2 on the circuit board, and then layer 5 (corresponding to applicant's layer 78) on the bottom side of the circuit board over resist 4. Layer 5 is deposited by a non-electrolytic plating method (see example, step 3; referred to in example, step 5 as deposited by electroless deposition). As shown in applicant's figure 4H, layer 78 is used to conduct electric current from an external power source to circuit patterns used as a power connection portion (as recited in the second step of claims 2, 9 and 19). Hirobumi et al performs the same step. As described in step 6), paragraph [0016] and shown in figure 5 (described in example, step 6), non-electrolytic layer 5 is used to conduct electric current from the cathode of the electroplating power source to circuit patterns used as a power connection portion.

8. At page 12 of the Remarks, applicant argue that Hirobumi et al do not disclose or suggest removing a portion of the photoresist to expose the connection pads and some of the circuit patterns to form a power connection portion, or coating a conductive layer on the surface of the substrate for connecting between the power connection portion and the external source.

Hirobumi et al shows openings in resist 4 to expose a connection pad and a portion of a circuit to form a power connection. As explained in the paragraph above, non-electrolytic copper layer 5 of Hirobumi et al corresponds to conductive layer 78 of applicant for connecting between the power connection portion and an external power source.

Art Unit: 1742

9. Applicant's arguments at pages 13 and 14 of the Remarks with regard to the rejection of the claims under 35 U.S.C. 103 are essentially the same as those directed to the rejection under 35 U.S.C. 102 which have been addressed above. While the Office Action Summary of the previous action indicated that claim 19 was rejected, applicant correctly notes that claim 19 was not specifically included in the detailed discussion of the rejection. The limitations of claim 19 are similar to those of the other claims addressed in the previous action, and the rationale for the rejection of claim 19 was, as indicated above, the same.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

Art Unit: 1742

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WL

William Leader  
May 25, 2007

ROY KING   
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 1700